**TCES 312 Analog Electronic**

**Lab 2: Common Emitter Amplifier**

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1. **Overview**

The purpose of the lab is to create a BJT common emitter amplifier using B2 Spice and by using a breadboard along with various complementary hardware pieces such as resistors, capacitors, and a transistor. Designing the circuit on B2 Spice is to help show that designing the circuit on the breadboard was done correctly. This lab is also used to show what changes from altering a few input variables by redesigning the circuit on B2 Spice.

The fluke multi-meter and the oscilloscope are two other pieces of hardware that are used during this experiment. The multi-meter is used to measure the node voltages with the DC bias currents and the oscilloscope is used to determine the peak-to-peak amplitude that represents the some AC parameters.

1. **Circuit schematic and explanation of its characteristics and operation**

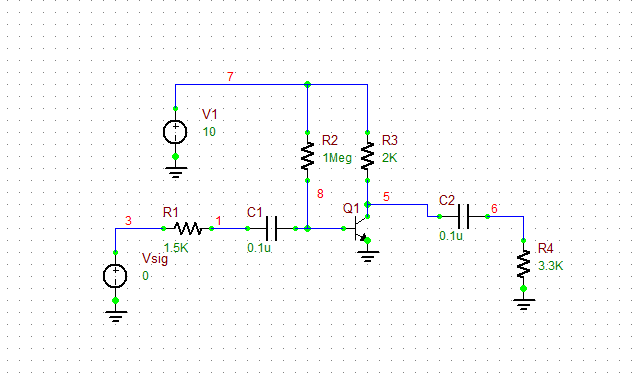


Figure 1: The original simulation circuit

Figure 1 shows a common emitter amplifier, created using resistors, capacitors, two voltage sources, and a transistor. This amplifier is supposed to increase the output voltage of an AC signal. The input voltage of the AC signal is represented by the voltage source labeled Vsig. The signals output voltage is increased by a certain amount, Aoverall, which can be determined by doing an AC sweep test on the above circuit on the B2 Spice program. Running the AC sweep test will result in a graph such as the one given in Figure 2. The redesign of this circuit increases R2 and R3 by a factor of two.

1. **Data and Analysis**

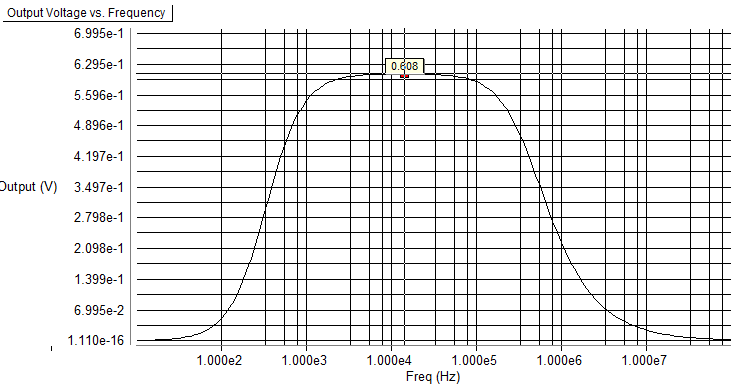
The data gathered in the table in Figure 3 was collected in a few different ways. The voltages for both simulations are collected by running a DC bias test. The voltages for the actual circuit that was made on the breadboard were collected by using a voltmeter. The voltage gains (A) for the simulations were collected by using the AC sweep test. Using the AC sweep test provided us with a graph such as the one on the next page labeled Graph 1. The voltage gain was determined by finding the output voltage (the maxima of the graph) and then dividing it by the input voltage (10 mV).

The gains for the actual circuit were collected using the oscilloscope and a series of equations. In order to find the different voltage gains, we need the original input voltage which was found by finding the difference between the minimum and maximum of the sinusoidal wave on the oscilloscope (∆Y) and then multiplying that by the voltage divider. An example of which is given on the next page under Example Calculation. In order to find each of the gains, the ∆Y’s of each sinusoidal wave were found and then divided by the input voltage. Now to find Rin and Rout, Av1 and Av2 had to be used along with specific equations. Both those equations are given on the next page under Equation 1 and Equation 2 respectfully.

Example Calculation: = input voltage.

Equation 1: To find =

Equation 2: To find : =

Figure 2: Overall gain of the circuit

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Original Simulation** | **Actual (Breadboard)** | **Redesign Simulation** |
|  | 0 | 0 | 0 |
|  | 0 | 0 | 0 |
|  | 5.945 | 5.97 | 5.96 |
|  | 0 | 0 | 0 |
|  | 10 | 9.95 | 10 |
|  | 0.645 | 0.651 | 0.627 |
|  |  |  |  |
|  | 60.8 | 57.6 | 54.0 |
|  | 146.4 | 141.6 | 147.2 |
|  | 96.03 | 92.09 | 116.4 |
|  | 92.79 | 88.22 | 68.32 |
| (kΩ) | 2.86 | 2.81 | 5.67 |
| (kΩ) | 1.91 | 1.98 | 3.81 |

Figure 3: The collected data table of simulations

1. **Conclusion**

In conclusion, the actual measurements made when the circuit was implemented on a breadboard were very close to those measurements made using the B2 Spice simulation, which was expected. While they are not perfect match-ups, being close to the simulated values is extremely important and indicates that the experiment was performed correctly. The redesign measurements show that increasing the resistance of R2 and R3 (RB and RC) by a factor of two increased the values of the input and output resistances by almost a factor of two as well.